CLAIMS

1. A semiconductor test apparatus characterized by comprising:

a first time interpolator to which clocks output from a device under test are input and which obtains the clocks by a plurality of strobes having constant timing intervals and which outputs the clocks as time-sequential level data;

a second time interpolator to which output data output from the device under test are input and which obtains the output data by a plurality of strobes having constant timing intervals and which outputs the output data as time-sequential level data; and

a first selection circuit which receives the time-sequential level data output from the first and second time interpolators, thereby selecting the output data input to the second time interpolator at edge timing of the clocks input to the first time interpolator, and outputting the selected data as measurement data of the device under test,

the first and/or second time interpolator being equipped with an edge selector to which the time-sequential level data obtained by the plurality of strobes are input and which selectively outputs level data indicating timing of rising edges and/or falling edges of the level data.

2. The semiconductor test apparatus according to claim 1, further comprising a second selection circuit

which receives the time-sequential level data output from the first time interpolator, thereby selecting the clocks input to the first time interpolator at edge timing of the clocks input to the first time interpolator, and outputting the selected clocks as clock data of the device under test.

3. A semiconductor test apparatus characterized by comprising:

a first time interpolator to which clocks output from a device under test are input and which obtains the clocks by a plurality of strobes having constant timing intervals and which outputs the clocks as time-sequential level data; and

a second selection circuit which receives the time-sequential level data output from the first time interpolator, thereby selecting the clocks input to the first time interpolator at edge timing of the clocks input to the first time interpolator, and outputting the clocks as clock data of the device under test,

the first time interpolator being equipped with an edge selector to which the time-sequential level data obtained by the plurality of strobes are input and which selectively outputs level data indicating timing of rising edges and/or falling edges of the level data.

4. The semiconductor test apparatus according to any one of claims 1 to 3, wherein the first time interpolator comprises:

a plurality of sequential logic circuits to which

the clocks output from the device under test are input;

a delay circuit which sequentially inputs strobes delayed at constant timing intervals to the plurality of sequential logic circuits and which outputs the time-sequential level data from the sequential logic circuits;

an edge selector to which the time-sequential level data output from the plurality of sequential logic circuits are input and which outputs level data indicating a rising edge, level data indicating a falling edge, or level data indicating rising and falling edges among the time-sequential level data obtained by inputting the clocks of the device under test; and

an encoder to which the level data output from the edge selector is input and which encodes the level data as timing data indicating edge timing of the clocks of the device under test and which outputs the timing data.

5. The semiconductor test apparatus according to claim 1 or 2, wherein the second time interpolator comprises:

a plurality of sequential logic circuits to which the output data output from the device under test are input; and

a delay circuit which sequentially inputs strobes delayed at constant timing intervals to the plurality of sequential logic circuits and which outputs the time-sequential level data from the sequential logic circuits.

6. The semiconductor test apparatus according to

claim 5, wherein the second time interpolator comprises:

an edge selector to which the time-sequential level data output from the plurality of sequential logic circuits are input and which outputs level data indicating a rising edge, level data indicating a falling edge, or level data indicating rising and falling edges among the time-sequential level data obtained by inputting the output data of the device under test; and

an encoder to which the level data output from the edge selector is input and which encodes the level data as timing data indicating edge timing of the output data of the device under test and which outputs the timing data.

7. The semiconductor test apparatus according to any one of claims 4 to 6, wherein the edge selector comprises:

one or more selector circuits comprising a first AND circuit to which an inverted output of one sequential logic circuit and a non-inverted output of a next-stage sequential logic circuit are input, a second AND circuit to which a non-inverted output of one sequential logic circuit and an inverted output of a next-stage sequential logic circuit are input, an OR circuit to which outputs of the first and second AND circuits are input, and a selector which selects one of outputs of the first and second AND circuits and the OR circuits.

8. The semiconductor test apparatus according to claim 1 or 2, wherein the first selection circuit

comprises: a selector which selects one data among the time-sequential level data input from the second time interpolator by using the time-sequential level data encoded by the first time interpolator as selection signals and which outputs the selected data as measurement data of the device under test.

9. The semiconductor test apparatus according to claim 2 or 3, wherein the second selection circuit comprises:

a selector which selects one data among the time-sequential level data input from the first time interpolator by using the time-sequential level data encoded by the first time interpolator as selection signals and which outputs the selected data as clock data of the device under test.

10. The semiconductor test apparatus according to claim 1 or 2, further comprising a bus which interconnects the first and second time interpolators and which distributes data output from the first and second time interpolators to predetermined selection circuits.